In The Claims:

Claim 1. (Original) An apparatus for improving IDE bus cable configuration detection, comprising:

a general-purpose input/output (GPIO) controller having at least one signal detection terminal for detecting IDE bus cable configuration; and

a D-type flip-flop having a triggering terminal, a clear terminal, an output terminal and a data input terminal, wherein said triggering terminal couples with a signal pin of said IDE bus, said output terminal couples with said signal detection terminal of said GPIO controller, said clear terminal couples with a system reset terminal and said data input terminal couples to a terminal having a high potential;

wherein said clear terminal can be triggered by a system reset so that said output terminal of said D-type flip-flop is reset to a low potential, and when said triggering terminal of said D-type flip-flop receives any signal variation, said output terminal of said D-type flip-flop outputs a high potential; and

when said output terminal of said D-type flip-flop outputs a low potential to said signal detection terminal of said GPIO controller, said IDE bus is diagnosed as one having an 80-pin cable configuration, and when said output terminal of said D-type flip-flop outputs a high potential to said signal detection terminal, said IDE bus is diagnosed as having a 40-pin cable configuration.

Claim 2. (Original) A latching device for linking between a detection device and an IDE bus, wherein said latching device has a triggering terminal, a clear terminal and an output terminal, said triggering terminal couples with a signal lead of said IDE bus and said output terminal couples with a signal detection terminal of said detection device;

said clear terminal can be triggered by a system reset so that said output terminal of said latching device is reset to a low potential, and when said triggering terminal of said latching device receives any signal variation, said output terminal of said latching device outputs a high potential;

when said output terminal of said latching device outputs a low potential to a signal detection terminal of said detection device, said IDE bus is diagnosed as having an 80-pin cable configuration, and when said output terminal of said D-type flip-flop outputs a high potential to said signal detection terminal, said IDE bus is diagnosed as having a 40-pin cable configuration.

Claim 3. (Original) The latching device of claim 2, wherein said latching device is a D-type flip-flop having a clear terminal and a data input terminal such that said clear terminal couples with a system reset terminal and said data input terminal couples with a terminal having a high potential.

Claim 4. (Original) The latching device of claim 2, wherein said detection device includes a general-purpose input/output (GPIO) controller.

Claim 5. (Original) The latching device of claim 2, wherein said detection device includes an integrated drive electronic (IDE) interface controller.

Claim 6. (Currently Amended) An apparatus for improving IDE bus cable configuration detection that links up a detection device and an IDE bus, comprising:

at least one latching device, wherein said latching device has a triggering terminal and an output terminal, said triggering terminal couples with a configuration diagnostic signal lead of said IDE bus and said output terminal couples with a signal detection terminal of said detection device, wherein said latching device further includes a clear terminal such that said output terminal of said latching device is reset to a low potential when said clear terminal is triggered by a system reset signal.

Claim 7. (Original) The apparatus of claim 6, wherein said latching device is a D-type flip-flop having a clear terminal and a data input terminal such that said clear terminal couples with a system reset terminal and said data input terminal couples with a terminal having a high potential.

Claim 8. (Original) The apparatus of claim 6, wherein said detection device includes a general-purpose input/output (GPIO) controller.

Claim 9. (Original) The apparatus of claim 6, wherein said detection device includes an integrated drive electronics (IDE) interface controller.

Claim 10. (Original) The apparatus of claim 6, wherein said IDE bus can have an 80-pin connection or a 40-pin connection.

Claim 11. (Original) The apparatus of claim 10, wherein said IDE bus is diagnosed as one having an 80-pin cable by said detection device if said output terminal of said latching device outputs a low potential to said signal detection terminal of said detection device.

Claim 12. (Original) The apparatus of claim 10, wherein said IDE bus is diagnosed as one having a 40-pin cable by said detection device if said output terminal of said latching device outputs a high potential to said signal detection terminal of said detection device.

Claim 13. (Canceled)

Claim 14. (Currently Amended) The apparatus of claim [[13]]6, wherein said output terminal of said latching device outputs a high potential when said triggering terminal of said latching device receives any signal variation.

Claim 15. (Original) An apparatus for improving IDE bus cable configuration detection, comprising:

a general purpose input/output (GPIO) controller having:

a detection device having at least one of signal detection terminal for detecting IDE bus cable configuration; and

a plurality of latching devices connected to said IDE bus cable and said detection device; wherein each said latching device has a triggering terminal, a clear terminal and an output terminal, said triggering terminal coupling with a signal lead of said IDE bus; said clear terminal triggered by a system reset so that said output terminal of said latching device is reset to a low potential, and when said triggering terminal of said latching device receives any signal variation, said output terminal of said latching device outputs a high potential,

wherein when said output terminal of said latching device outputs a low potential to said signal detection terminal of said detection device, said IDE bus is diagnosed as having an 80-pin cable configuration, and when said output terminal of said latching device outputs a high potential, aid IDE bus is diagnosed as having a 40-pin cable configuration.